UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,931,505 B2
DATED : August 16, 2005
INVENTOR(S) : David

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9,
Line 7, delete "tage" and insert -- tag --.
Lines 10-11, delete ", the command sequencer and serializer unit to control the data cache located on the memory module".
Line 12, after "lines," insert -- each of --.
Line 13, before "sequentially" insert -- including a plurality of segments --.
Line 14, at the end delete "command" and insert -- segment --.
Line 15, after "periods," insert -- wherein --.
Line 16, delete "including" and insert -- include --.
Line 16, at the end after "command" insert -- to read data from a memory device of the memory module --.
Line 17, after "cache fetch command" insert -- to fetch data from the data cache of the memory module --.
Line 20, after "transfer periods" insert -- , while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical --.
Line 59, after "memory bus" delete ", the memory controller component including an array of tag address storage locations --.
Line 61, before "the commands" insert -- each of --.
Line 61, after "the commands" insert -- including a plurality of segments --.
Line 63, after "transaction" insert -- and each of the segments being delivered within one of the transfer periods --.
Line 63, before "the plurality" insert -- wherein --.
Line 63, after "of commands" delete "including" and insert -- include --.
Line 63, after "activate command" insert -- to read data from the at least one memory device --.
Line 64, after the second occurrence of "command" insert -- to fetch data from the data cache --.
Line 68, after "periods" insert -- ,while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical. --.

Column 10,
Line 27, after "controller," insert -- each of --.
Line 27, after "commands" insert -- including a plurality of segments --.
Line 29, after "transaction" insert -- and each of the segments being delivered within one of the transfer periods, wherein --.
Line 30, delete "including" and insert -- include --.
Line 30, after "command" insert -- to read data from the at least one memory device --.
Line 31, after "command," insert -- to fetch data from the data cache --.

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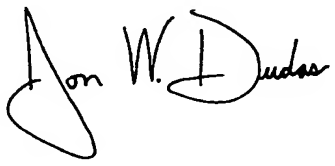
Column 10 (cont'd),
Line 34, after "periods" insert -- ,while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical. --.
Line 64, after "command," insert -- while a remainder of the segments of the activate command and the cache fetch command transferred during transfer periods other than the last transfer period remains substantially identical. --.

Column 12,
Line 5, after "command" insert -- ,while a remainder of the segments of the read command and the read and preload command transferred during transfer periods other than the last transfer period remains substantially identical. --.

Signed and Sealed this

Twenty-eighth Day of February, 2006



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